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Nuclear Physics B (Proc. Suppl.) 156 (2006) 252–256
NUCLEAR PHYSICS B PROCEEDINGS SUPPLEMENTS
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BTeV Trigger

Erik E. Gottschalk [a]
For the BTeV Collaboration

[a]Fermi National Accelerator Laboratory, Batavia, IL 60510, U.S.A.

BTeV was designed to conduct precision studies of CP violation in $B\overline{B}$ events using a forward-geometry detector in a hadron collider. The detector was optimized for high-rate detection of beauty and charm particles produced in collisions between protons and antiprotons. The trigger was designed to take advantage of the main difference between events with beauty and charm particles and more typical hadronic events—the presence of detached beauty and charm decay vertices. The first stage of the BTeV trigger was to receive data from a pixel vertex detector, reconstruct tracks and vertices for every beam crossing, reject at least 98% of beam crossings in which neither beauty nor charm particles were produced, and trigger on beauty events with high efficiency. An overview of the trigger design and its evolution to include commodity networking and computing components is presented.

1. INTRODUCTION

Future trigger and data acquisition systems for experimental high energy physics and nuclear physics experiments are expected to face challenges that are similar to those confronted by BTeV. The challenge is to design complex triggers that achieve high efficiency for physics of interest while maintaining high levels of background rejection in a high-rate environment. The BTeV trigger system was designed to meet this challenge. The design of the trigger system evolved over time as changes were made to the design of the detector, as physics and detector simulations improved, and in response to numerous technical, cost and schedule reviews. For example, the final change that was made to the baseline design of the trigger entailed a significant reduction in cost and schedule risk, and a proposed design change was expected to further reduce the cost while enhancing scalability and fault tolerance aspects of the trigger. Unfortunately, BTeV was cancelled on February 7, 2005 after successfully passing critical reviews [1]. However, the design concepts that were developed for BTeV over many years should be applicable to future experiments facing similar challenges.

2. THE BTEV EXPERIMENT AND SPECTROMETER

The primary goal of the BTeV experiment was to acquire as many $B\overline{B}$ events as possible so that subtle differences between B and $\overline{B}$ mesons could be studied. BTeV was designed to operate in the C0 interaction region of the Tevatron at Fermilab at a luminosity of 2×10^{32} cm^{-2} s^{-1}, corresponding to an average of six interactions per beam crossing at a crossing rate of 2.5 MHz. BTeV was going to benefit from the large $b\overline{b}$ cross section at the Tevatron $(\sigma(b\overline{b}) \sim 100\mu b)$ and take advantage of the unique characteristics of hadronic b production in the forward region [2], [3].

The design of the BTeV spectrometer [4] was optimized for the forward region and consisted of tracking detectors and particle-identification detectors. For particle identification BTeV had a muon detector, a Ring Imaging Cherenkov (RICH) detector, and a lead-tungstate ($PbWO_4$) electromagnetic calorimeter. For tracking BTeV had a silicon-pixel detector, silicon microstrips, and straw-tube chambers. The silicon-pixel detector was the centerpiece of the spectrometer and consisted of 30 planar tracking stations centered on the C0

0920-5632/$ – see front matter
doi:10.1016/j.nuclphysbps.2006.02.124

interaction region and immersed in a 1.5 Tesla dipole magnet. Each pixel station had more than 7.6 × 10^5 individual pixels, for a total of more than 22 × 10^6 pixels in the entire detector. Individual pixels were rectangular, with a dimension of 50 × 400 μm^2. The data from the pixel detector were to be used in the first stage of the BTeV trigger, Level 1.

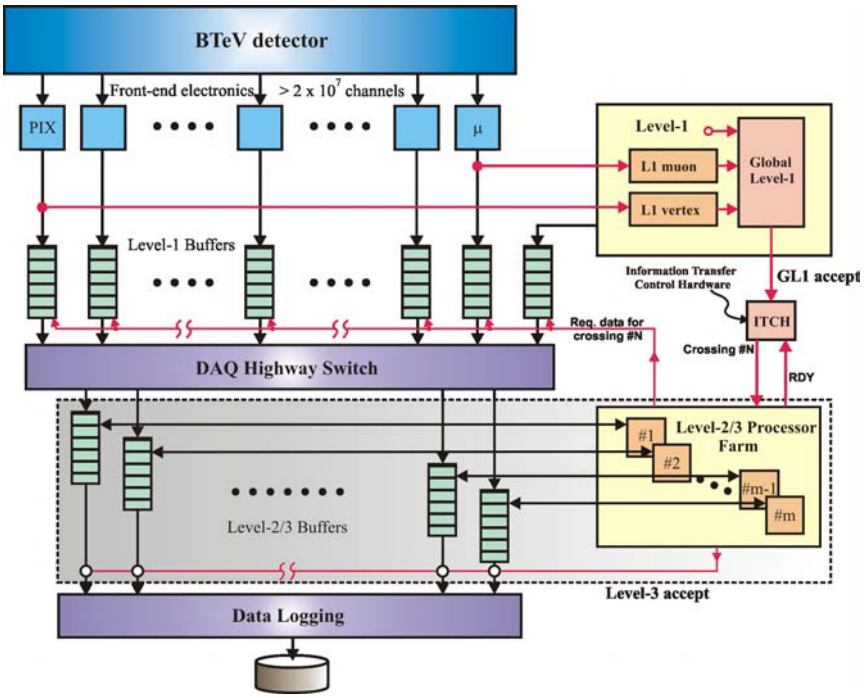

Figure 1. BTeV three-level trigger architecture. Front-end electronics send data to Level-1 buffers, where the data are held while pixel and muon data are processed by the Level-1 trigger. Data that pass Level 1 are sent to Level 2/3 by sending data from the buffers to Level 2/3 through a commodity DAQ highway switch. Data that pass Level 2/3 are archived to disk using commodity hardware.

3. OVERVIEW OF THE BTEV TRIGGER

The BTeV trigger was designed to identify *B* mesons by their decay properties. At Tevatron energies *B* mesons decay after traveling a distance of a few millimeters relative to the $p\bar{p}$ collision point, where they are produced. To trigger on *B* mesons the BTeV trigger system was designed to analyze data from every beam crossing in order to find the tracks of *B* decay products in beam crossings with multiple interactions and high track multiplicities. The system was designed to trigger on rarely produced *B* mesons (~ 1/500 $p\bar{p}$ collisions produce *B*'s at the Tevatron) with high efficiency, while rejecting more typical background interactions that do not produce *B* mesons.

The BTeV trigger was designed as a three-level hierarchical trigger system (shown in Fig. 1) that is typical for many High Energy Physics (HEP) experiments [5]. Each trigger level in the hierarchy reduces the data rate, so that subsequent trigger levels have more time to perform more detailed analyses of the data. For BTeV the lowest level trigger, which is referred to as Level 1 (L1), was to examine data from the pixel detector for every beam crossing to find events with *B* mesons while data from all other detector systems were temporarily saved in buffers, referred to as "Level-1 buffers" or "L1 buffers." L1 was designed to reduce the input crossing rate by a factor of 50, resulting in an input rate into the Level 2/3 trigger (L2/3) of 50 kHz. L2/3, which was to be implemented on a farm of commodity PC's, was to perform a more detailed analysis of events using data from other detector systems by reading the data from L1 buffers. The processing that was to be performed by L2/3 corresponded to the CPU-intensive event reconstruction that is traditionally performed as

"offline analysis" in other HEP experiments. L2/3 was to reduce the rate by another factor of 20, which would have resulted in an output rate of 2.5 kHz written to archival storage.

What distinguished the BTeV trigger from trigger systems in other HEP experiments was the amount of processing that was going to be applied at L1 so that sophisticated algorithms performing track and vertex reconstruction in the first level trigger could be used. This is unlike other HEP experiments that are forced to use fast, but primitive, algorithms on custom-built hardware for the lowest trigger levels due to time constraints imposed on the trigger and data acquisition hardware.

BTeV's L1 trigger was designed to be free of severe time constraints due to the asynchronous nature of its data acquisition (DAQ) system in which data from all detector systems were to be read out at the beam crossing rate of 2.5 MHz and stored in very large L1 buffers built with low cost commodity DRAM [6]. The design of the BTeV DAQ made it practical to achieve a memory capacity corresponding to three orders of magnitude more storage time compared to the average L1 latency, thereby enabling the processing of every beam crossing at L1.

A simplified block diagram of BTeV's L1 trigger is shown in Fig. 2. The diagram shows that pre-processed pixel data from three adjacent pixel tracking stations are sent to FPGA (Field Programmable Gate Array) segment finders that perform necessary pattern recognition to find beginning and ending track segments (called "triplets") in the pixel detector. Since individual segment-finder hardware modules operate on a

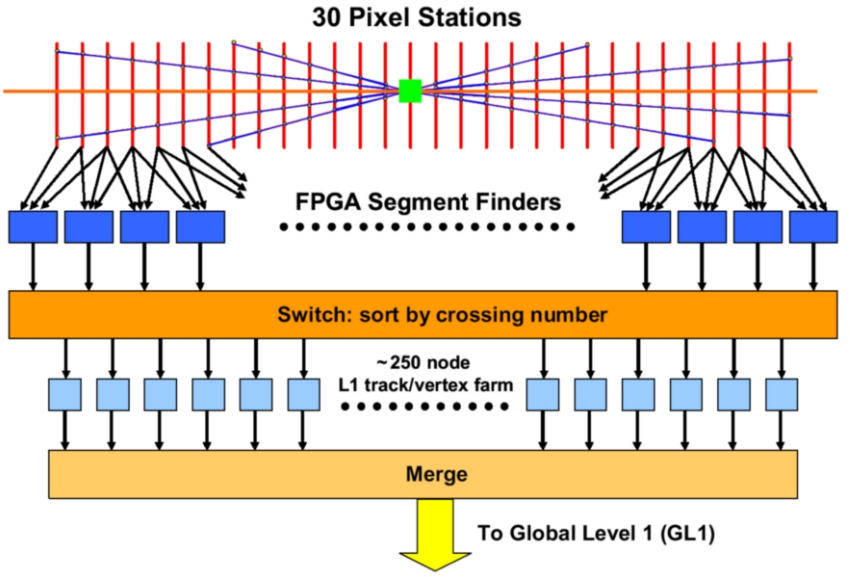

Figure 2. BTeV Level 1 trigger. Data from silicon pixel tracking stations are read out and processed by FPGA hardware. FPGA segment finders reconstruct 3-station track segments that are sorted by crossing number using a switch that directs all track segments for a single crossing to a processor in the L1 track/vertex farm. L1 pixel trigger results are merged with L1 muon trigger (not shown) results and sent to Global Level 1 (not shown). Global Level 1 uses the combined results to produce the trigger decision for L1 for each beam crossing.

subset of the data from the pixel detector, all triplets associated with the same beam crossing are routed through an event-building switch to a single processor in the L1 track/vertex farm. This farm performs the second stage of L1 trigger calculations by matching the beginning and ending track segments so that complete tracks are reconstructed. The tracks are then used to reconstruct primary interaction vertices. Tracks that are found to be "detached" from primary vertices are tagged as possible candidates for tracks from *B* decays. These results along with primary vertex locations are sent to the Global Level 1 trigger, which makes the final

trigger decision for L1. If at least two detached tracks that meet certain criteria are associated with a particular primary vertex, then the event satisfies L1 trigger conditions and is sent to L2/3. A more detailed description of the L1 algorithm and BTeV trigger architecture can be found in Refs. [7] and [8].

4. BASELINE CHANGES TO THE BTEV TRIGGER ARCHITECTURE

The original baseline design of the L1 trigger consisted of custom-designed hardware that included an event-building switch and processor farm that was to be built with several thousand digital signal processors (DSPs). A prototype system was built using 150 MHz Texas Instruments TMS320C6711 DSPs [9]. Considerable effort went into determining benchmarks for the L1 trigger code on these DSPs, as well as running the code on processors ranging from System-On-a-Chip (SOC) hardware to general purpose processors used in desktop PCs [10]. After determining these benchmarks, we concluded that general-purpose processors were superior to the DSP hardware since the L1 trigger code ran at least an order of magnitude faster on the general-purpose processors. These results and other considerations that were based on cost, schedule, and risk analyses prompted us to replace the original baseline design with a design that included more commodity computing and networking hardware. The choices that were made for a prototype system replaced the custom event-building switch in the baseline design with an Infiniband switch [11], and replaced the DSP farm with a farm of Apple Xserves [12].

Although the change from custom-built hardware to commodity hardware represented a significant change to the L1 trigger (including a significant reduction in cost), it did not represent a fundamental change in the architecture of the trigger system. A second change to the new baseline design of the L1 trigger was expected to simplify the trigger and reduce the cost even further. This baseline change was underway when the BTeV Project was canceled [1].

The second baseline change was going to integrate the function performed by the event-building switch (see Fig. 2) into the FPGA pixel pre-processing and segment-finder hardware. The design was referred to as the "integrated upstream event builder" (IUEB) [13], [14]. The change was considered to be technically feasible because the event-building switch performed a time-stamp ordering for pixel data that was also one of the functions performed by the pixel pre-processing hardware.

Advantages of the IUEB included the following. First, since individual segment finders were going to receive data from the entire pixel detector, the number of segment-finder modules would be independent of detector geometry and could be scaled to satisfy trigger performance characteristics. Second, the IUEB was going to introduce a greater degree of fault tolerance in the segment-finder hardware compared to the original baseline design. Third, the IUEB could allow increased optimization of the L1 trigger by offloading CPU-intensive operations (for example, track reconstruction) from the L1 processor farm to FPGA hardware, which could also allow optimization of the L2/3 trigger by moving L2/3 operations into L1. Other advantages of the IUEB proposal such as more efficient use of network bandwidth and the introduction of commodity blade-server hardware are presented elsewhere [14].

5. CONCLUSION

The BTeV trigger system was designed to trigger on $B\overline{B}$ events in the demanding environment of a hadron-collider experiment. The design was based on commodity processors, memory, and networking components for a substantial part of the system. The trigger design is unique in the amount of processing applied at the lowest level, Level 1. An important feature of the data acquisition system is the asynchronous readout, which is based on large

buffers built with commodity DRAM. Modifying the trigger design to replace custom-built DSP hardware with general-purpose processors simplified the hardware design, introduced hardware that was easier to program, and resulted in significantly less cost for material and labor while reducing schedule risks for BTeV. Furthermore, a proposed change to modify the baseline trigger architecture by using an "integrated upstream event builder" promised to enhance the scalability and fault-tolerance of the trigger system while further reducing the cost of the system. We believe that the design of the BTeV trigger can serve as a model for future experiments that will be confronted with similar challenges of complex triggering in high-rate environments.

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